REF35 Ultra Low-Power, High-Precision Voltage Reference

1 Features

- Ultra-low quiescent current:
  - 680 nA (typical)
- Initial accuracy: ±0.05% (maximum)
- Temperature coefficient:
  - 10 ppm/°C (maximum for −40°C to 125°C)
- Output 1/f noise (0.1 Hz to 10 Hz): 8.5 ppm_{P-P}
- NR pin to reduce noise
- EN pin to reduce shutdown current consumption
- Excellent long-term stability: 20 ppm @ 1k hr
- Excellent thermal hysteresis: 20 ppm
- Specified temperature range: −40°C to +125°C
- Operating temperature range: −55°C to +125°C
- Output current: +10 mA, −5 mA
- Input voltage: V_{REF} + V_{DO} to 6 V
- Output voltage options:
  - 1.024 V, 1.2 V, 1.25 V, 1.6 V, 1.8 V, 2.048 V, 2.5 V, 3.0 V, 3.3 V, 4.096 V, 5.0 V
- Small footprint 6-pin SOT−23 package

2 Applications

- Flow transmitter
- Blood glucose monitor
- Servo drive control module
- Power quality analyzer
- Fault indicator
- Oscilloscope
- Process analytics

3 Description

The REF35 is a family of nanopower, low-drift, high-precision series reference devices. The REF35 family features high ±0.05 % initial accuracy with power consumption typically below 700 nA. The low temperature drift (10 ppm/°C) and long-term drift (20 ppm @ 1000 hrs) ensures system stability and reliability. The low power consumption combined with high precision specifications are suitable for wide variety of portable and low current applications.

The REF35 supplies up to 10 mA current with 8.5 ppm_{p-p} noise and 30 ppm/mA load regulation. With this feature set, REF35 creates a strong low-noise high accuracy power supply for precision sensors and 12–16b data converters.

The family is fully specified for operation from -40°C to 125°C and is functional over -55°C to 125°C. The wide temperature is suited for industrial applications.

REF35 is available in wide output voltage variants starting from 1.024 V to 5.0 V. The device is offered in space saving SOT23-6 pin package. Contact the TI sales representative for additional voltage options.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
REF35xxx	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available voltage variants and packages, see the orderable addendum at the end of the data sheet.

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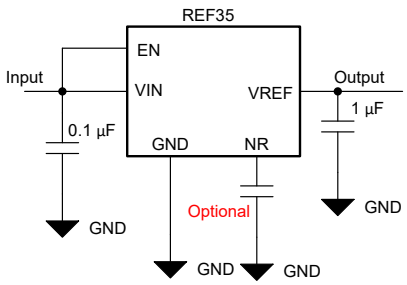
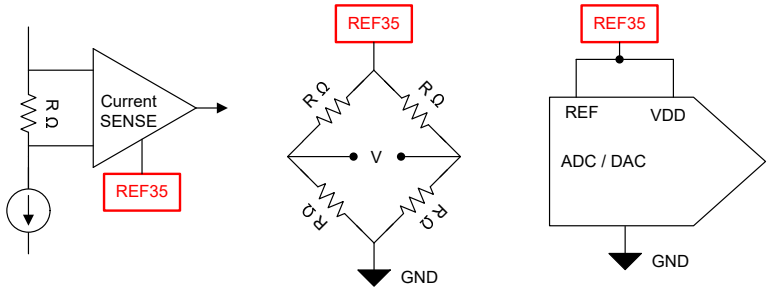
Connection Diagram



Typical Application Use Cases



Amplifier Biasing
CSA, INA, DFA etc

Sensor power supply
Bridge, Thermocouple etc

Data Converter power supply

REF35 Use Case

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Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2021	*	Initial APL Release

5 Device Comparison Table

PRODUCT	V_{REF}
REF35102	1.024 V
REF35120	1.2 V
REF35125	1.25 V
REF35160	1.6 V
REF35180	1.8 V
REF35205	2.048 V
REF35250	2.5 V
REF35300	3.0 V
REF35330	3.3 V
REF35409	4.096 V
REF35500	5.0 V

6 Pin Configuration and Functions

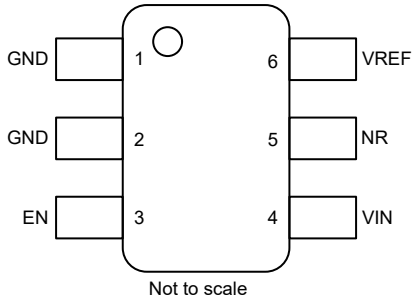

Figure 6-1. Package
6-Pin DBV
Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DGK		
GND	1	Ground	Device ground connection
GND	2	Ground	Device ground connection
EN	3	Input	Enable connection. Enables or disables the device.
VIN	4	Power	Input supply voltage connection
NR	5	Output	Noise reduction pin. Connect a capacitor to reduce noise.
VREF	6	Output	Reference voltage output

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	IN	–0.3	6.5	V
Enable voltage	EN	–0.3	IN + 0.3 (2)	V
Output voltage	V_{REF}	–0.3	IN + 0.3 (2)	V
Output short circuit current	I_{SC}		20	mA
Operating temperature range	T_A	–55	125	°C
Storage temperature range	T_{stg}	–65	170	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.
(2) IN + 0.3 V or 6.5 V, whichever is lower

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Input voltage (1)	V_{OUT} + V_{DO} (2)		6	V
EN	Enable voltage	0		IN	V
I_L	Output current	–5		10	mA
T_A	Operating temperature	–40	25	125	°C

(1) For V_{REF} = 1.024 V to 1.5 V, mimimum V_{IN} = 1.7 V
(2) V_{DO} = Dropout voltage

7.4 Thermal Information

THERMAL METRIC(1)		DEVICE DBV (SOT23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	164.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	102.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	44.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	59.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At V_{IN} = V_{REF} + 0.5 V, V_{EN} = V_{IN}, C_{REF} = 10 µF, C_{IN} = 0.1 µF, I_L = 0 mA, minimum and maximum specifications at T_A = –40°C to 125°C, typical specifications T_A = 25°C; unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	T_A = 25°C		–0.05		0.05	%
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 85°C				TBD	ppm/°C
		–40°C ≤ T_A ≤ 125°C				10	ppm/°C
LINE AND LOAD REGULATION							
$\Delta V_{REF}/\Delta V_{IN}$	Line regulation	V_{REF} < 2.5 V; V_{IN} = V_{REF} + V_{DO} to V_{INMAX}			4	160	ppm/V
		V_{REF} ≥ 2.5 V; V_{IN} = V_{REF} + V_{DO} to V_{INMAX}			4	80	ppm/V
$\Delta V_{REF}/\Delta I_L$	Load regulation	I_L = 0 mA to 10 mA, V_{IN} = V_{REF} + V_{DO}	Source		20	60	ppm/mA
		I_L = 0 mA to 5 mA, V_{IN} = V_{REF} + V_{DO}	Sink		40	150	ppm/mA
POWER SUPPLY							
V_{IN}	Input voltage (1)			V_{REF} + V_{DO}		6	V
I_Q	Quiescent current	Active mode	T_A = 25°C		0.68	1	µA
			–40°C ≤ T_A ≤ 85°C			1.3	
			–40°C ≤ T_A ≤ 125°C			2.6	
		Shutdown mode	T_A = 25°C			0.05	
			–40°C ≤ T_A ≤ 125°C			1.2	
V_{EN}	Enable pin voltage	Active mode (EN = 1 or Float)		0.7 x V_{IN}			V
		Shutdown mode (EN = 0)				0.3 x V_{IN}	
I_{EN}	Enable pin current	V_{EN} = V_{IN}			0.1	0.3	uA
V_{DO}	Dropout voltage	I_L = 5 mA				250	mV
		I_L = 10 mA				500	
I_{SC}	Short circuit current, Sourcing	V_{REF} = 0 V, T_A = 25°C			30	35	mA
		V_{REF} = 0 V				20	
	Short circuit current, Sinking	V_{REF} = V_{IN} V, T_A = 25°C			18	20	mA
		V_{REF} = V_{IN} V				14	
TURNON TIME							
t_{ON}	Turn-on time (2)	0.1% settling, C_{REF} = 1 µF, V_{REF} = 2.048 V			2		ms
NOISE							
e_n	Output voltage noise	f = 10 Hz to 1 kHz			32		ppm_{rms}
e_{np-p}	Low frequency noise	f = 0.1 Hz to 10 Hz, V_{REF} ≥ 2.5 V			8.5		ppm_{p-p}
		f = 0.1 Hz to 10 Hz, V_{REF} < 2.5 V			10		ppm_{p-p}
HYSTERESIS AND LONG-TERM STABILITY							
	Long-term stability	0 to 1000h at 35°C			20		ppm
	Output voltage hysteresis	25°C, –40°C, 125°C, 25°C (cycle 1)			20		ppm
STABLE CAPACITANCE RANGE							
	Input capacitor range			0.1			µF
	Output capacitor range (3)			0.1		10	µF

(1) For V_{REF} = 1.024 V to 1.5 V, mimimum V_{IN} = 1.7 V
(2) Scales linearly with V_{REF}.
(3) ESR for the capacitor can range from 10 mΩ to 400 mΩ

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7.6 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

Figure 7-1. Output Voltage Vs Free-Air Temperature (V_{REF} = 1.25 V)

Figure 7-2. Output Voltage Vs Free-Air Temperature (V_{REF} = 2.5 V)

Figure 7-3. Output Voltage Vs Free-Air Temperature (V_{REF} = 5.0 V)

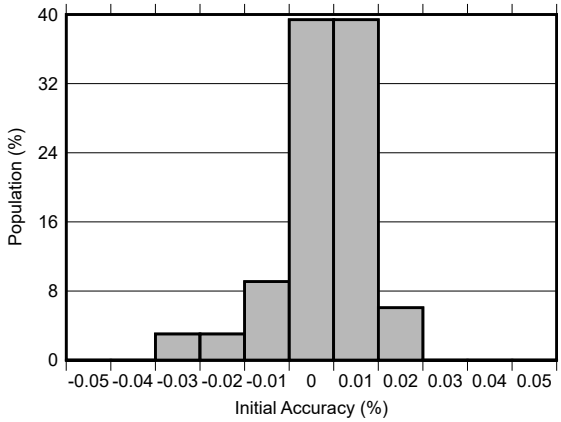

Figure 7-4. Initial Accuracy Distribution

Figure 7-5. Temperature Coefficient Distribution (-40ºC to 125ºC)

Figure 7-6. Temperature Coefficient Distribution (-40ºC to 85ºC)

Figure 7-7. Load Regulation (Sourcing 10 mA) Vs Free-Air Temperature

Figure 7-8. Load Regulation (Sinking 5 mA) Vs Free-Air Temperature

Figure 7-9. Load Transient Response (C_L = 10 µF)

Figure 7-10. Load Transient Response (C_L = 0.1 µF)

Figure 7-11. Line Regulation Vs Free-Air Temperature

Figure 7-12. Line Transient Response

Figure 7-13. Output Impedance

Figure 7-14. Quiescent Current Vs Free-Air Temperature

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Figure 7-15. Shutdown Current Vs Free-Air Temperature

Figure 7-16. Dropout Voltage Vs Free-Air Temperature

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8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF35 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 32 devices were soldered on two printed circuit boards [16 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 8-1. The printed circuit board is comprised of FR4 material. The board thickness is TBD mm and the area is TBD mm × TBD mm.

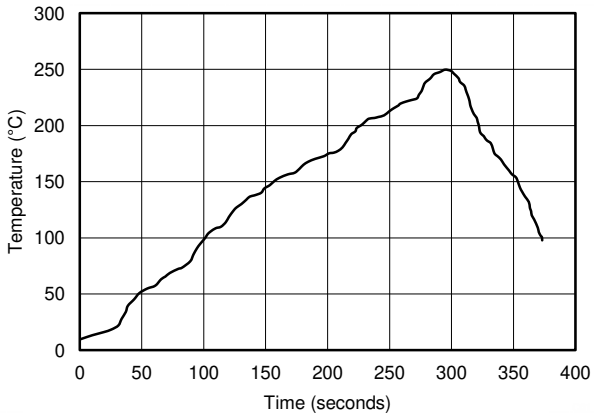

Figure 8-1. Reflow Profile

The reference output voltage is measured before and after the reflow process; the typical shift is displayed in Figure 8-2. Although all tested units exhibit very low shifts (< TBD%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the last pass to minimize its exposure to thermal stress.

Figure 8-2. Solder Heat Shift Distribution, V_{REF} (%)

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8.2 Temperature Coefficient

The REF35 is designed and tested for a low output voltage temperature coefficient, which is defined as the change in output voltage over temperature. The temperature coefficient is calculated using the box method in which a box is formed by the min/max limits for the nominal output voltage over the operating temperature range. REF35 has a low maximum temperature coefficient of 10 ppm/°C from –40°C to +125°C and TBD ppm/°C from –40°C to +85°C. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. Due to temperature curvature correction to achieve low-temperature drift, the temperature drift is expected to be non-linear. See *SLYT183* for more information on the box method. The box method equation is shown in Equation 1

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(25°C)} \times \text{Temperature Range}} \right) \times 10^6 \quad (1)$$

Figure 8-3 shows a typical voltage versus temperature curves across 32 devices. Figure 8-4 shows the distribution of temperature coefficients across 32 devices.

Figure 8-3. Output Voltage Vs Free-Air Temperature

Figure 8-4. Temperature Coefficient Distribution

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8.3 Long-Term Stability

One of the key performance parameters of the REF35 references is long-term stability also known as long-term drift. The long-term stability value is tested in a typical setup that reflects standard PCB board manufacturing practices. The boards are made of standard FR4 material and the board does not have special cuts or grooves around the devices to relieve the mechanical stress of the PCB. The devices and boards in this test do not undergo high temperature burn in post-soldering prior to testing. These conditions reflect a real world use case scenario and common manufacturing techniques.

During the long-term stability testing, precautions are taken to ensure that only the long-term stability drift is being measured. The boards are maintained at 35°C in an oil bath. The oil bath ensures that the temperature is constant across the device over time compared to an air oven. The measurements are captured every 30 minutes with a calibrated 8.5 digit multimeter.

Typical long-term stability characteristic is expressed as deviation of reference voltage output over time.

Figure 8-5 shows the typical drift value for the REF35 in SOT23-6 package is TBD ppm from 0 to 1000 hours. It is important to understand that long-term stability is not ensured by design and that the value is typical. The REF35 will experience the highest drift in the initial 1000 hr. Subsequent deviation is typically lower than first 1000 hr.

Figure 8-5. Long Term Stability - 1000 hours (V_{REF})

8.4 Thermal Hysteresis

Thermal hysteresis is measured with the REF35 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. The PCB was baked at 150°C for 30 minutes before thermal hysteresis was measured. Hysteresis can be expressed by Equation 2:

$$V_{HYST} = \left(\frac{| V_{PRE} - V_{POST} |}{V_{NOM}} \right) \times 10^6 \text{ (ppm)} \quad (2)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to +125°C and returns to 25°C.

Typical thermal hysteresis distribution is as shown in Figure 8-6.

Figure 8-6. Thermal Hysteresis Distribution (V_{REF})

8.5 Noise Performance

The reference pin output noise is categorized as low frequency and broadband noise. Following sections describe these categories in detail.

8.5.1 Low Frequency (1/f) Noise

Flicker noise, also known as 1/f noise, is a low frequency noise that affects the device output voltage which can affect precision measurements in ADCs. This noise increases proportionally with output voltage and operating temperature. It is measured by filtering the output from 0.1-Hz to 10-Hz. Since the 1/f noise is an extremely low value, the frequency of interest needs to be amplified and band-pass filtered. This is done by using a high-pass filter to block the DC voltage. The resulting noise is then amplified by a gain of 1000. The bandpass filter is created by a series of high-pass and low-pass filter that adds additional gain to make it more visible on a oscilloscope as shown in Figure 8-7. Figure 8-8 shows the effect of flicker noise over 10 second. Flicker noise must be tested in a Faraday cage enclosure to block environmental noise.

Figure 8-7. Low Frequency (1/f) Noise Test Setup

Figure 8-8. 0.1-Hz to 10-Hz Voltage Noise

Figure 8-9 shows the typical 1/f noise (0.1-Hz to 10-Hz) distribution across REF35 devices. REF35 device also offers noise reduction functionality by adding an optional capacitor between NR (pin 5) and ground pins.

Figure 8-10 shows the typical 1/f noise (0.1-Hz to 10-Hz) distribution across REF35 devices with 10 µF capacitor between NR pin and GND.

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Figure 8-9. 0.1-Hz to 10-Hz Noise Distribution (NR = Open)

Figure 8-10. 0.1-Hz to 10-Hz Noise Distribution (NR = 10 µF)

8.5.2 Broadband Noise

Broadband noise is a noise that appears at higher frequency compared to 1/f noise. The broadband noise is measured by high-pass filtering the output of the reference device, followed by a gain stage and measuring the result on a spectrum analyzer as shown in Figure 8-11

Figure 8-11. Broadband Noise Test Setup

For noise sensitive designs, a low-pass filter can be used to reduce broadband noise output noise levels by removing the high frequency components. When designing a low-pass filter special care must be taken to ensure the output impedance of the filter does not degrade ac performance. This can occur in RC low-pass filters where a large series resistance can impact the load transients due to output current fluctuations. The REF35 device also offers noise reduction functionality by adding an option capacitor between NR (pin 5) and ground pins. Figure 8-12 shows the noise spectrum for REF35 device when NR pin is open. Figure 8-13 shows the noise spectrum for REF35 device when 10 µF capacitor is connected between NR pin and GND.

Figure 8-12. Noise Spectrum 10 Hz to 100 kHz (NR = Open)

Figure 8-13. Noise Spectrum 10 Hz to 100 kHz (NR = 10 µF)

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8.6 Power Dissipation

The REF35 voltage references are capable of source up to 10 mA and sink up to 5 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with Equation 3:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (3)$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

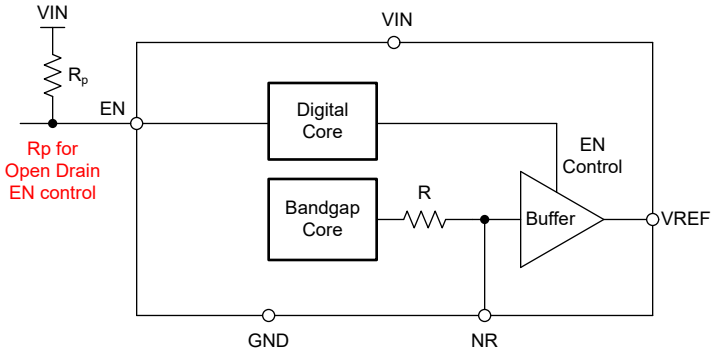
Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the device be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

9 Detailed Description

9.1 Overview

The REF35 is family of ultralow current, low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The *Functional Block Diagram* is a simplified block diagram of the REF35 showing basic band-gap topology.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Supply Voltage

The REF35 family of references features an extremely low dropout voltage. For 10 mA loaded conditions, a maximum dropout voltage is 500 mV. Figure 7-16 shows a typical dropout voltage (V_{DO}) versus load current. The device supports operation with input voltage range from V_{REF} + V_{DO} to 6 V. The typical quiescent current is 680 nA and maximum quiescent current over temperature is only 2.6 µA. The low dropout voltage coupled with ultral-ow current enable the operation across multiple battery powered applications.

9.3.2 EN Pin

The REF35 family supports device enable and disable functionality through logic level control on EN pin. The EN pin of REF35 does not use an internal pull-up resistor. Instead, it uses a new 'clean EN' technology. This allows EN pin to left floating and at the same time no extra current is drawn from the supply when EN pin is pulled low in shut-down mode. When EN pin is pulled high or left unconnected, the device is in active mode. When EN pin is drive by an open-drain outputs, a pull-up resistor to VIN is required. The device must be in active mode for normal operation. The EN pin must not be pulled higher than VIN supply voltage.

The device can be placed in shutdown mode by pulling the EN pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device drops to 50 nA.

It is to be noted that for applications where EN pin is left floating, total parasitic capacitance on EN pin should be restricted within 30 pF.

See the Section 7.5 for logic high and logic low voltage levels.

9.3.3 NR Pin

The REF35 pin allows access to the bandgap through the NR pin. Placing a capacitor from the NR pin to GND creates a low-pass filter in combination with the internal resistance R. Leakage of the capacitance directly impacts the accuracy and temperature drift. If NR functionality is used, choose a low leakage capacitor. A capacitance of 1 µF creates a low-pass filter with corner frequency around TBD Hz. Such a filter decreases the overall noise on the VREF pin. Higher capacitance results in a lower filter cut off frequency, further reducing output noise. Please note, using the capacitor on NR pin also increases start-up time.

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9.4 Device Functional Modes

9.4.1 Basic Connections

Figure 9-1 shows the typical connections for the REF35. TI recommends a supply bypass capacitor (C_{IN}) ranging from 0.1 µF to 10 µF. A 1 µF to 10 µF output capacitor (C_L) must be connected from REF to GND. The equivalent series resistance (ESR) value of C_L must be between TBD mΩ to TBD mΩ to ensure output stability.

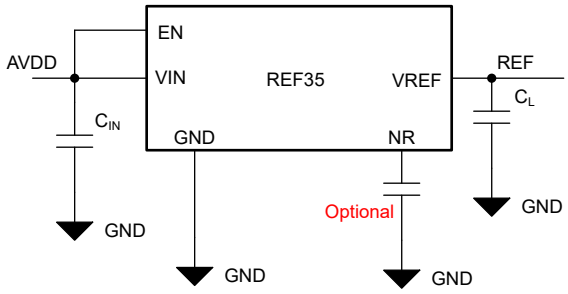

Figure 9-1. Basic Connections

9.4.2 Start-Up

Figure 9-2 shows the start-up behavior of REF35205 device with 1 µF load capacitance. REF35 device ensures the output voltage settles to the expected output voltage within specified accuracy without oscillations. The start-up time is dependent on the output voltage variant, output capacitance and NR pin capacitance. Higher capcitance leads to longer start-up time.

Figure 9-2. REF35205 Start-up Behavior, C_{REF} = 1 µF

9.4.3 Output Transient Behavior

The REF35 output buffer is capable of sourcing 10 mA load current as well as sink 5 mA of load current. The output stage is designed using class B architecture to achieve low quiescent current. This architecture has a cross over dead band close to no load condition. Any load transient where the load current is close to dead band will require wider settling time. The settling time will be higher for large output capacitor. For larger load steps e.g. ADC reference drive the settling time will be faster.

Figure 9-3 and Figure 9-4 show the output settling behavior for light load transient and high load transient respectively.

Figure 9-3. Load Transient Response 0 µA to 100 µA, C_{REF} = 1 µF

Figure 9-4. Load Transient Response 1 mA to 10 mA, C_{REF} = 1 µF

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

REF35 with low current consumption and class leading performance specifcations is suitable reference for multiple applications. The device can also be used as a precision low noise power supply to sensor or data converter instead of traditional LDO or DC/DC based power supply. Basic applications includes positive/negative voltage reference and data acquisition systems. The table below shows the typical application of REF35 and its companion ADC/DAC.

Table 10-1. Typical Applications and Companion ADC/DAC

APPLICATIONS	ADC/DAC
PLC - DCS	ADS7028, DAC8881, ADS1287, ADS7953
Rack Server	ADS7028, ADS7128, ADS7138
Field Transmitters - Pressure, Flow	ADS124S08
Optical Module, Optical Line Card	ADS7068, ADS7138
Medical Blood Glucose Meter	ADS1112

10.2 Typical Application: Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF35 and OPA735 can be used to provide a dual-supply reference from a 5-V supply. Figure 10-1 shows the REF35250 used to provide a 2.5-V supply reference voltage. The low drift performance of the REF35250 complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R1 and R2.

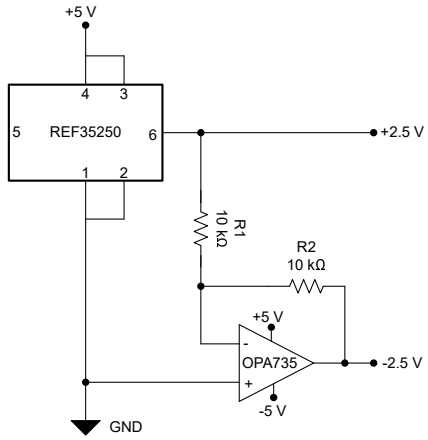

Figure 10-1. REF35 and OPA735 Create Positive and Negative Reference Voltages

10.3 Typical Application: Precision Power Supply and Reference

Figure 10-2 shows the basic configuration for the REF35 device as precision power supply to ADS7038 data converter which uses its power supply AVDD as reference. Connect bypass capacitors according to the guidelines in Section 10.3.2.2 section.

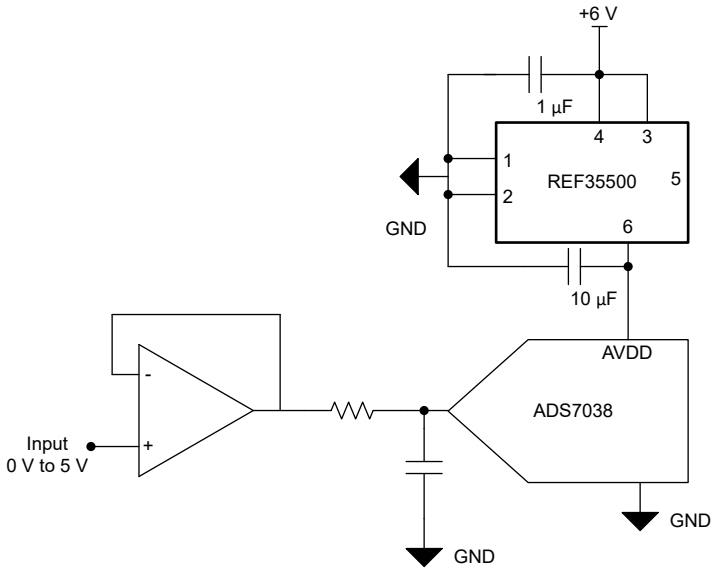

Figure 10-2. Basic Reference Connection

10.3.1 Design Requirements

A detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 10-2 as the input parameters.

Table 10-2. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage range V_{IN}	0 V - 5 V
Output resolution	12-bit
REF35 input capacitor	1 µF
REF35 output capacitor	10 µF

10.3.2 Detailed Design Procedure

10.3.2.1 Selection of Reference

REF35500 reference is selected for this design. REF35500 device operates of very low quiescent current while offering ±0.05 % initial accuracy and very low temperature drift. These parameters help improve system accuracy as compared to external LDO based power supply. The 5 V reference voltage supports the 0 V to 5 V input range specification.

10.3.2.2 Input and Output Capacitors

A 1-µF to 10-µF electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. Connect an additional 0.1-µF ceramic capacitor in parallel to reduce high frequency supply noise.

A ceramic capacitor of at least a 0.1 µF must be connected to the output to improve stability and help filter out high frequency noise. Add an additional 10-µF electrolytic or ceramic capacitor in parallel to improve transient performance in response to sudden changes in load current; however, keep in mind that doing so increases the start-up time of the device.

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Best performance and stability is attained with low-ESR, low-inductance ceramic chip-type output capacitors (X5R, X7R, or similar). If using an electrolytic capacitor on the output, place a 0.1-µF ceramic capacitor in parallel to reduce overall ESR on the output.

10.3.2.3 Selection of ADC

ADS7038 12-bit 8 channel multiplexed ADC is chosen for this application. The ADC offers low current operation with averaging mode to increase the resolution to 16-bit with internal averaging modes while operating with slow sampling speed.

10.3.3 Application Curves

Table 10-3 shows the captured measurement results for various DC inputs. The ADC output is captured and analyzed for output accuracy, code spread and sigma with REF35500 as power supply vs LDO as power supply.

Table 10-3. DC Input Performance Test Results

INPUT V	REF35500			LDO		
	MEASURED V	CODE SPREAD	SIGMA	MEASURED V	CODE SPREAD	SIGMA
1.0 V	TBD V	TBD	TBD	TBD V	TBD	TBD
2.5 V	TBD V	TBD	TBD	TBD V	TBD	TBD
4 V	TBD V	TBD	TBD	TBD V	TBD	TBD

11 Power Supply Recommendations

The REF35 family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage at no load. TI recommends a supply bypass capacitor ranging between 0.1 µF to 10 µF.

12 Layout

12.1 Layout Guidelines

Figure 12-1 illustrates an example of a PCB layout for a data acquisition system using the REF35. Some key considerations are:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors at V_{IN}, V_{REF} of the REF35.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

Figure 12-2 illustrates pin compatibility with TI REF30xx, REF31xx and REF33xx series references in SOT23-3 package when using REF35xxx family footprint. Key is to rotate the REF30xx, REF31xx and REF33xx reference devices by 180º before assembly.

12.2 Layout Example

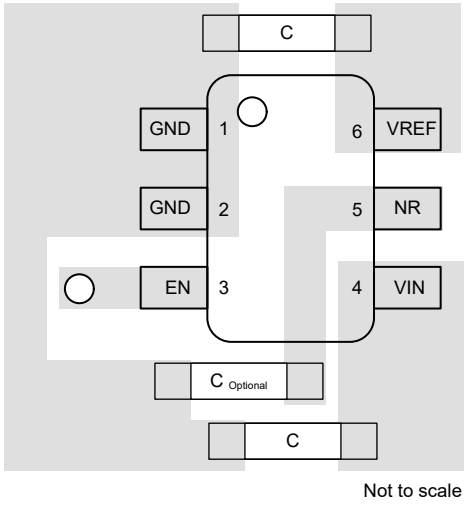

Figure 12-1. Layout Example

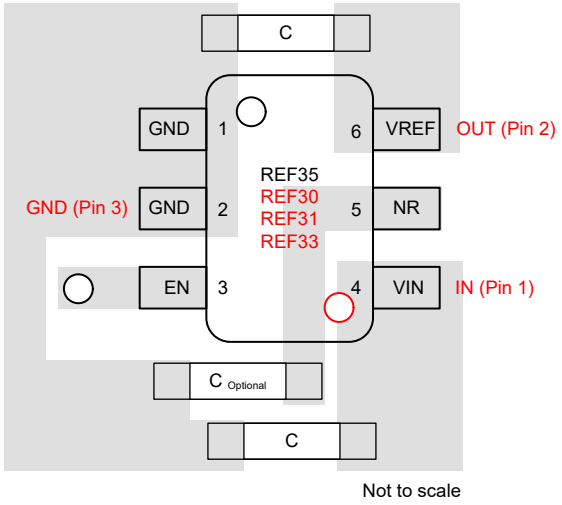

Figure 12-2. Pin Compatibility with REF30xx, REF31xx and REF33xx

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors*
- *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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